



25805610

QP CODE: 25805610

Reg No :

Name :

M.C.A. DEGREE EXAMINATION, NOVEMBER 2025

First Semester

Faculty of Technology & Applied Science

Master of Computer Application

CORE - MCACT102 - DIGITAL LOGIC & COMPUTER ORGANIZATION

2020 Admission Onwards

DF1DCF7E

Time: 3 Hours

Maximum: 75 Marks

Part A

*Answer any **ten** questions*

*Each question carries **3** marks*

1. Add the binary numbers 11011101 and 111011.
2. Differentiate between check sum and parity scheme.
3. Encode data bits 1101 into the 7 bit even parity Hamming code .
4. Apply DeMorgan's theorem to the expression $(A + B + C)D'$.
5. Write the steps to convert SOP into standard SOP. Give example.
6. How is a register different from shift register?
7. State the principle of operation of a carry look-ahead adder.
8. What is control memory?
9. State Locality of Reference for cache memory.
10. Explain Virtual Memory.
11. Explain the need for interconnection networks in multiprocessor systems.
12. What is meant by instruction pipelining?

(10×3=30 marks)





Part B

Answer *all* questions

Each question carries 9 marks

13. a) Explain the rules for the following (i) Binary Addition; (ii) Binary Subtraction. Give examples.

OR

- b) Explain the working of 7 bit hamming code with an example

14. a) Reduce the Boolean expression $[AB' (C + BD) + A'B'] C$ as much as possible using algebraic method.

OR

- b) Explain the four types of shift registers.

15. a) With a diagram, explain the components of a computer.

OR

- b) Explain Booth Algorithm with an example.

16. a) Explain Cache memory and its advantages.

OR

- b) Explain Direct Memory Access with suitable diagrams.

17. a) Explain in detail the following SIMD parallel structures: Array Processors, Vector Processors.

OR

- b) Explain the interconnection structures used in multiprocessors .

(5×9=45 marks)

