



QP CODE: 25050700



25050700

Reg No :

Name :

MSc DEGREE (CSS) EXAMINATION DECEMBER 2025

First Semester

M.Sc APPLIED ELECTRONICS

Core Courses - EL020103 - DIGITAL SYSTEM DESIGN

2019 Admission Onwards

2D22DDF5

Time: 3 Hours

Weightage: 30

Part A (Short Answer Questions)

*Answer any **eight** questions.*

*Weight **1** each.*

1. Define Duality Theorem.
2. What do you mean by Don't care Terms.
3. Briefly explain timing diagram with example.
4. Discuss state reduction in digital systems.
5. Explain finite state model.
6. What do you mean by critical race? How can we overcome this?
7. Compare PLA and PAL.
8. Explain about an FPGA.
9. Write note on the Simulation tools in HDL.
10. Define Entity in VHDL.

(8×1=8 weightage)

Part B (Short Essay/Problems)

*Answer any **six** questions.*

*Weight **2** each.*

11. How can we reduce equation using POS method?
12. Explain the SOP Method of K -Map reduction technique.
13. What are the design steps in synchronous circuit design?
14. Explain State diagram, State table and state Assignment.
15. Explain the capabilities and limitations of FSM.





16. What do you mean by machine minimization?
17. Explain shift and add multiplier.
18. Explain behavioural modelling and mention its advantages.

(6×2=12 weightage)

Part C (Essay Type Questions)

*Answer any **two** questions.*

Weight 5 each.

19. Compare K Map and Quine McCuskey methods of minimisation with example.
20. Design a four bit synchronous up counter with state diagram.
21. Design Fundamental mode asynchronous counter without latch based on the following equations

$$Q_1 t = X_1 \overline{X_2} + \overline{X_1} + X_2 Q_2 + X_2 Q_1 \overline{Q_2}$$

$$Q_2 t = \overline{X_1} X_2 \overline{Q_1} + X_1 Q_2 + X_2 Q_2$$

$$Y = X_1 \oplus Q_1 \oplus Q_2$$

22. Explain in detail Xilinx Spartan IIE FPGA.

(2×5=10 weightage)

