



QP CODE: 25047507



Reg No : .....

Name : .....

**M.Sc DEGREE (CSS) EXAMINATION, NOVEMBER 2025**

**Third Semester**

M Sc ELECTRONICS

**Core Course - EL010301 - DIGITAL SYSTEM DESIGN**

2019 ADMISSION ONWARDS

28A2CCF1

Time: 3 Hours

Weightage: 30

**Part A (Short Answer Questions)**

*Answer any **eight** questions.*

*Weight 1 each.*

1. Is full adder a combinational circuit ? Why ?
2. Convert the decimal 395 to BCD.
3. Convert the BCD 0010 0111(decimal 27) to binary.
4. Draw a switching element with inputs x1, output Y, weight 4,threshold value -2.
5. What is the difference between flip flop and a latch?
6. Give the block diagram of a serial -in -serial -out shift register.
7. What are the peculiarities of a Mealy state machine?
8. What is Merger Graph?
9. Define an entity in VHDL.
10. Give two examples for basic identifiers.

(8×1=8 weightage)

**Part B (Short Essay/Problems)**

*Answer any **six** questions.*

*Weight 2 each.*

11. Draw the block diagram and explain a 4x1 multiplexer. Give the truth table.
12. Describe a 2 line 4line decoder.
13. Explain how we can convert SR to D?
14. Define (i) Strongly connected machine? (ii) state equivalence theorem?
15. Explain minimal closed covering?





16. Distinguish between package declaration and package body.
17. Describe different multiplying operators in VHDL?
18. Describe the Behavioral style of modelling.

(6×2=12 weightage)

**Part C (Essay Type Questions)**

*Answer any **two** questions.*

*Weight 5 each.*

19. Minimise the function using Quine Mc Cluskey tabular method,  $f(W,X,Y,Z) = \sum m (2,6,8,9,10,11,14,15)$ .
20. Design a 3 bit asynchronous up down counter.
21. Explain the features and capabilities of VHDL in detail.
22. Design a NAND gate using Structural modelling.

(2×5=10 weightage)

