23104820

QP CODE: 23104820

Reg No : .....

Name : .....

B.Sc DEGREE (CBCS) REGULAR/IMPROVEMENT/REAPPEARANCE EXAMINATIONS, FEBRUARY 2023

First Semester

Complementary Course - EL1CMT06 - ELECTRONICS - FUNDAMENTALS OF DIGITAL SYSTEMS

(Common to B.Sc Cyber Forensic Model III, B.Sc Computer Science Model III)

2017 Admission Onwards

930E8C65

Time: 3 Hours Max. Marks : 80

Part A

*Answer any **ten** questions.*

*Each question carries **2** marks.*

1. What weight does the digit 7 have in each of the following numbers?
   (a) 1370 (b) 6725 (c) 7051 (d) 58.72
2. Find the binary and decial equivalent of F7A9116.
3. Find the Octal and decimal equivalent of 110110112.
4. Describe the pecuilarity of ASCII code.
5. Develop the truth table for a 3-input AND and ORgate.
6. Define an XOR and an XNOR gate.
7. State associative law for boolean addition.
8. Define race around condition.
9. (a) What is the purpose of a clock input to a flip flop?
   (b) When does an invalid state occur in an SR Latch?
10. What are master slave flip flops?
11. Give a description of universal shift registers.
12. Explain how a Johnsons counter differ from a ring counter?

(10×2=20)

Part B

*Answer any **six** questions.*

*Each question carries **5** marks.*

13. Find the decimal equivalent of the following binary numbers.
    (a) 111011.11 (b) 10010.11011 (c) 1101110 (d) 1111.110
14. Express AND-OR logic using relevant logic circuit and expressions.
15. Implement the expression
    (a) X=((A'+B'+C')DE)' by using NAND logic (b) X= ((A'B'C'+(D+E))' using NOR logic.
16. Realize the Basic gates using NAND and NOR gates.
17. Write a note on boolean addition and multiplication.
18. Convert the expression (A+B'+C)(B'+C+D')(A+B'+C'+D) to standard POS form.
19. Develop a timing diagram and combinational logic circuit for the function X(=A(B+C))'
20. Give any four comparison between synchronous and asynchronous counters.
21. Design a 4-bit synchronous decade counter.

(6×5=30)

Part C

*Answer any **two** questions.*

*Each question carries **15** marks.*

22. With suitable examples
    (a) explain the methods for implementing signed arithmetic
    (b) explain floating point numbers in signed binary arithmetic.
23. Using Boolean algebrae techniques simplify the following expressions and implement using logic gates of both before and after simplification
    (a) AB+A(B+C)+B(B+C) (b) (AB+AC)'+A'B'C (c) AB'C(BD+CDE)+AC'
24. With relevant figures explain a (a) priority BCD encoder (b) 8X1 MUX.
25. With neat diagram explain the working of
    (a) a four bit serial in serial out shift register (b) Parallel in parallel out shift register.

(2×15=30)