QP CODE: 24027880

24027880

Reg No : .....

Name : .....

B.Sc DEGREE (CBCS) REGULAR / IMPROVEMENT / REAPPEARANCE EXAMINATIONS, OCTOBER 2024

Third Semester

B.Sc Cyber Forensic Model III

Core Course - CF3CRT08 - MICROPROCESSORS

2019 Admission Onwards

B8126238

Time: 3 Hours Max. Marks : 80

Part A

*Answer any **ten** questions.*

*Each question carries **2** marks.*

1. What is the use of flag register?
2. What is primary memory?
3. Write any two Data transfer instruction.
4. What is the use of RET instructions?
5. What is the structure for if-then-else programs?
6. What is a procedure?
7. What is the meant by indirect far CALL?
8. What is the function of PUSH instruction?
9. Define divide by zero interrupt.
10. What is priority interrupt controller?
11. Explain protected mode of operation.
12. Write down the concept of RISC System.

(10×2=20)

Part B

*Answer any **six** questions.*

*Each question carries **5** marks.*

13. Explain the I/O reads and I/O write operations of 8085.

14. List out the various signals used in 8085.

15. Explain the BIU of 8086 microprocessor .

16. Explain string instructions used in the 8086 processor.

17. Differentiate re-entrant and recursive procedures.

18. What happen when 8253 is used as a timing and delay generation peripheral?

19. Describe software triggered strobe.

20. What are the functions of the signals ‘processor extension request(PEREQ)’ and ‘PEACK’ in 80286 processors?

21. Explain the cache memory of 80486.

(6×5=30)

Part C

*Answer any **two** questions.*

*Each question carries **15** marks.*

22. a. Explain the various peripheral initiated operations of 8085. b. Draw and explain the timing diagram of an instruction fetch operation of 8085 microprocessor.

23. Explain with example the addressing modes of 8086 microprocessor.

24. Draw and explain the timing diagram for DMA transfer.

25. Draw and discuss internal architecture of 80386 in detail.

(2×15=30)