QP CODE: 24019922

24019922

Reg No : .....

Name : .....

B.Sc DEGREE (CBCS) REGULAR / IMPROVEMENT / REAPPEARANCE EXAMINATIONS, MAY 2024

Second Semester

Core Course - EL2CRT05 - DIGITAL ELECTRONICS

(Common for B.Sc Electronics and Computer Maintenance Model III, B.Sc Electronics Model III)

2017 ADMISSION ONWARDS

7B2B8EF9

Time: 3 Hours Max. Marks : 80

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Part A

*Answer any **ten** questions.*

*Each question carries **2** marks.*

1. Convert the following gray code to binary : (a) 1010 (b) 00110.
2. Express OR gate using NAND only.
3. Prove that A+A'B = A+B.
4. Expand TTL, DTL, ECL, IIL .
5. CMOS Logic gate is the combination of?
6. Draw the truth table of a half adder.
7. List the applications of a comparator.
8. Why is a demultiplexer called a data distributor?
9. What is a master slave flip flop?
10. How will you convert a 4 bit serial data in to 4 parallel data?
11. Describe a two bit binary counter using T flipflops.
12. What is the basic difference between pulse triggered and edge triggered flip flops?

(10×2=20)

Part B

*Answer any **six** questions.*

*Each question carries **5** marks.*

13. What is 2's compliment and its use? Give an example .

14. What is POS? Illustrate with suitable expression and logic gate implementation.

15. Why ECL logic gates are used for high frequency applications ?

16. Explain a binary to excess 3 code converter.

17. Explain different types of parity.

18. Distinguish between a combinational logic circuit and sequential logic circuit.

19. Describe the working of clocked SR flip flop.

20. Explain the concept of MOD 5 counter.

21. Expain the concept of MOD 10 counter.

(6×5=30)

Part C

*Answer any **two** questions.*

*Each question carries **15** marks.*

22. State and prove Demorgan's theorems using logic ciruits and truth tables.

23. Explain important characteristics of a logic family.

24. Discuss the working and applicatins of a 3 line to 8 line decoder.

25. Explain working of 4 bit negative edge triggered asynchronous counter.

(2×15=30)