QP CODE: 24020506

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Reg No : .....

Name : .....

B.Sc/BCA DEGREE (CBCS) REGULAR / IMPROVEMENT / REAPPEARANCE EXAMINATIONS, MAY 2024

Second Semester

Core Course - CS2CRT05 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Common for B.Sc Computer Science Model III, B.Sc Information Technology Model III, Bachelor of Computer Applications)

2017 ADMISSION ONWARDS

5B0A5BF1

Time: 3 Hours Max. Marks : 80

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Part A

*Answer any **ten** questions.*

*Each question carries **2** marks.*

1. What do you mean by the term immediate instruction?
2. What do you mean by a register?
3. What is two address instruction?
4. Define word length.
5. What is the purpose of using status registers?
6. Write about arithmetic instructions.
7. Write about branch instructions.
8. Write the use of bootstrap loader program.
9. What are the features of PROM?
10. What is page fault?
11. What is instruction stream?
12. What are hardware interlocks? How they are useful?

(10×2=20)

Part B

*Answer any **six** questions.*

*Each question carries **5** marks.*

13. Explain the basic components of digital computer.

14. Describe instruction cycle.

15. Explain about single bus structure with neat diagram.

16. Describe memory stack implementation.

17. Explain RAM. List various types.

18. What is the purpose of Cache Memory? Explain.

19. Describe address space and memory space.

20. Explain multi processing systems.

21. Write and explain the instruction format for vector processor.

(6×5=30)

Part C

*Answer any **two** questions.*

*Each question carries **15** marks.*

22. Explain various addressing modes, giving suitable examples for each.

23. Explain memory hierarchy.

24. Explain different parallel processing mechanisms in a uniprocessor system.

25. Explain pipeline conflicts and discuss the remedies for them.

(2×15=30)