QP CODE: 25019895

25019895

Reg No : .....

Name : .....

B.Sc DEGREE (CBCS)) REGULAR/ IMPROVEMENT/ REAPPEARANCE / MERCY CHANCE EXAMINATIONS, FEBRUARY 2025

Fourth Semester

B.Sc Information Technology Model III

Core Course - IT4CRT05 - PARALLEL PROCESSING

2017 Admission Onwards

937773A6

Time: 3 Hours Max. Marks : 80

Part A

*Answer any **ten** questions.*

*Each question carries **2** marks.*

1. Differentiate between floating point accelerator and diagnostic memory.
2. Define batch systems
3. Define the term bandwidth.
4. What is pipelining?
5. Define latency sequence.
6. Define array processors.
7. Define store -store overwriting.
8. Compare circuit switching and packet switching.
9. What do you know about the active or disabled PEs in SIMD array processors?
10. What do you meant by crossbar switch networks?
11. What is deadlock?
12. Define data flow graph.

(10×2=20)

Part B

*Answer any **six** questions.*

*Each question carries **5** marks.*

13. What do you know about array computers?

14. Compare and contrast between SISD and SIMD.

15. Write short notes on the three classes of data dependent hazards.

16. Compare the address increment and the address offset in vector processor.

17. What are the routing functions of Mesh connected networks?

18. What are tightly coupled and loosely coupled multiprocessor?

19. Give figure for crossbar switch system organization.

20. What are the major design issues of a data flow computer?

21. Illustrate and describe the structure of processing element in a data flow machine.

(6×5=30)

Part C

*Answer any **two** questions.*

*Each question carries **15** marks.*

22. Explain in detail about the multiprocessor systems.

23. Describe the design of pipelined instruction instruction units with necessary diagrams.

24. Explain about the multiprocessor operating systems.

25. Explain in detail about data-driven computing.

(2×15=30)