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Reg. No.....

Name.....

B.Sc. DEGREE (C.B.C.S.S.) EXAMINATION, SEPTEMBER 2024

First Semester

Complementary Course—DIGITAL ELECTRONICS

(Common for B.Sc. Electronics and B.Sc. Computer Maintenance and Electronics)

[2013—2016 Admissions]

Time : Three Hours

Maximum Marks : 80

Part A

*Answer **all** questions.*

Each question carries 1 mark.

1. 2's complement of 10010110 is _____.
2. BCD representation of 42.35 is _____.
3. Give the next three numbers : 4A5, 4A6, 4A7, 4A8 _____.
4. The XOR gate produces 1 at the output when _____.
5. In an RS flip-flop, when R = 0 and S = 0, the state _____.
6. In a JK flip-flop, when J = 1 and K = 1, the state _____.
7. ECL stands for _____.
8. How is synchronization achieved in digital circuits ?
9. What is a decade counter ?
10. State De Morgan's theorems.

(10 × 1 = 10)

Part B

*Answer any **eight** questions.*

Each question carries 2 marks.

11. Find the BCD and Gray code of 459.
12. Give the logic diagram and truth table of a 3 input XOR gate.

Turn over





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13. Prepare the truth table for the expression $(A + B) C$.
14. Mention the characteristics of TTL gates.
15. What do you understand by the term logic family ?
16. What is a half subtractor ? Obtain its truth table.
17. What is a latch ?
18. What is edge triggering ?
19. What is meant by race condition in flip-flops ?
20. What is a PIPO shift register ?
21. What are up/down counters ?
22. What are the disadvantages of asynchronous counters ?

(8 × 2 = 16)

Part C

*Answer any **six** questions.*

Each question carries 4 marks.

23. What is a full-adder ? Design a full-adder using basic logic gates.
24. Simplify using Boolean algebra.
 - (a) $A + AB$.
 - (b) $AB + AB'$.
 - (c) $A'BC + AC$.
 - (d) $A'B + ABC' + ABC$.
25. Using De Morgan's theorem show that :
 - (a) $(A + B)' (A' + B')' = 0$.
 - (b) $A + A'B + A'B' = 1$.
26. What are the factors deciding the fan-out, speed of operation, noise immunity and power dissipation in a logic family ?
27. Differentiate between RS and JK flip flops.





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28. What is a decoder ? What are its uses ?
29. Explain the behavior of a basic RS latch with active LOW inputs.
30. Explain the working of master slave flip flop.
31. Design a 2-bit asynchronous binary up/down counter. Explain its behaviour using a timing diagram of its counting sequence.

(6 × 4 = 24)

Part D

*Answer any **two** questions.*

Each question carries 15 marks.

32. Which are the Universal gates ? With examples show how each of these Universal gates can be used to implement other gates.
33. Simplify the Boolean function F together with the don't care conditions D in SOP form and POS form. $F(w, x, y, z) = \sum (0, 1, 2, 3, 7, 8, 10)$. $D(w, x, y, z) = \sum (5, 6, 11, 15)$.
34. What are multiplexers and demultiplexers ? Explain their functioning with examples.
35. Describe different types of shift registers.

(2 × 15 = 30)

