Model Question Paper
(Model I)

MAHATMA GANDHI UNIVERSITY

B.Sc. Physics Programme

V Semester Examination. ……..…….. (Month) ……..… (Year)

PH5B04U – DIGITAL ELECTRONICS

Instructions:

Time allotted: 3 hours

Answer all questions in part A. This contains 4 bunches of 4 objective questions. For each bunch, grade A will be awarded if all the 4 answers are correct, B for 3, C for 2, D for 1 and E for 0. Answer any 5 questions from part B, any 4 from part C and any 2 from part D. Candidates can use non-programmable calculators (ordinary/scientific) and/or tables.

Part A (Objective type – weight 1 each)

Bunch I

1. The decimal number (-39), when expressed as a signed binary in the sign-magnitude form is
   (a) 01011000 (b) 00100111 (c) 11011000 (d) 10100111
2. The binary equivalent and its 2's complement are the same for a decimal number, among the group of decimal numbers 8,9,10 & 11. Which one is it ?
   (a) 8 (b) 9 (c) 10 (d) 11.
3. Which of the following is not a valid rule of Boolean algebra?
   (a) A + 1 = 1 (b) A + 0 = 0 (c) A.A = A (d) A + 0 = A.
4. The Boolean expression AB + CD represents
   (a) two ORs ANDed together
   (b) a 4-input AND gate
   (c) two ANDs ORed together
   (d) an exclusive OR.

Bunch II

5. A 3-variable Karnaugh map has
   (a) sixteen cells (b) eight cells (c) four cells (d) three cells.
6. If $Y = (\overline{A} + B)(A + B)$, then

(a) Y = A (b) Y = B (c) Y = A + B (d) $Y = \overline{A} + B$

7. The logic gate which can be used as a comparator is
   (a) AND gate (b) XOR gate (c) NAND gate (d) XNOR gate.
8. If $F(A, B, C) = \sum(1,3,5)$, then $\overline{F}(A, B, C) =$
   (a) $\Pi(1,3,5)$ (b) $\Pi(0,2,4,6,7)$ (c) $\sum(1,3,5)$ (d) $\sum(0,2,4,6,7)$

Bunch III

9. Full adder is a combination of
   (a) 2 half adders
   (b) 2 half adders and an OR gate
   (c) 2 half adders and an AND gate
   (d) 2 half adders and a XOR gate.
10. Data selectors are basically the same as
    (a) decoder (b) demultiplexer (c) encoder (d) multiplexer.
11. For a T flip-flop, the output is
    (a) Always 0, when T=0 (b) always 0, when T=1
    (c) $Q_{n+1} = Q_n$, when T=0 (d) $Q_{n+1} = Q_n$ when T=1.
12. The number of CLK pulses required to write and read one byte of information in a SISO shift register is
    (a) 2 (b) 4 (c) 8 (d) 16.

Bunch IV

13. The number of flip-flops required for a decade counter is
    (a) 3 (b) 4 (c) 9 (d) 10.
14. The race-around problem does not occur in
    (a) SRFF (b) clocked SRFF (c) JKFF (d) MSJKFF
15. A JKFF with J = 1 and K = 1 has a 10 KHz clock input. The Q output is
    (a) constantly high (b) constantly low
    (c) a 10 KHz square wave (d) a 5 KHz square wave.
16. The percentage resolution of a D/A converter is determined by
    (a) the value of the resistors used in the R-2R ladder network
    (b) the total number of bits of the digital data input
    (c) the supply voltage
    (d) the number of 1's in the digital data input.

Part B (Short answer questions – weight 1 each)

17. What is an ASCII code? Give a short note on it.
18. Write the expression for a 3-input EXOR gate. Construct the complete truth table showing the outputs for all possible cases. Also draw the logic diagram.

19. What is meant by propagation delay? Mention a device which is used as a delay device.
20. Find the values of the variables that make each product term 1 and each sum term 0.
    (a)$A\overline{B}C$ (b)$\overline{A}B\overline{C}D$ (c)$\overline{A} + B + \overline{C}$ (d) $\overline{A} + \overline{B} + C + \overline{D}$
21. Describe the working of a half adder.
22. What is a MUX? Explain the difference between MUX and DEMUX.
23. What is meant by edge triggering? Give the difference between positive and negative edge triggering.
24. Distinguish between the performance of asynchronous and synchronous counters.

Part C (Short essay/Problems – weight 2 each)

25. Subtract the following numbers using 2's complement method.
    (a) + 47 – (+16) (b) +23 – (+65)
26. Apply DeMorgan's theorem to simplify the following expressions.
    (a) $\overline{A(B + C)}$ (b) $\overline{(A + \overline{B})(\overline{C} + D)}$
27. Use a Karnaugh map to simplify the following expression.
$$Y = ABCD + A\overline{B}\overline{C}\overline{D} + A\overline{B}C + AB$$
28. Design the logic diagram of a four bit adder-subtractor and explain its working.
29. What is meant by a decoder? Give the truth table and logic diagram of a binary to octal decoder.
30. Convert the following truth table to the corresponding Boolean expression using sum of products method.

Inputs			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Part D (Essay-type questions – weight 4 each)

31. State and explain DeMorgan's theorems Draw the logic circuits representing the theorems using basic gates. Prove the theorem for a 4-variable function.
32. Draw the logic diagram of a Master Slave JK flip-flop and explain its working.
33. Explain the working of a Digital to Analog converter using R-2R ladder network.