MAHATHMA GANDHI UNIVERSITY

Core 13 Microprocessor & Assembly Language Programming

Bsc Computer science III semester

MULTIPLE CHOICE QUESTIONS

1. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.
   A. multiple
   B. single
   C. double
   D. triple
   ANSWER: B

2. Microprocessor is a/an _____ circuit that functions as the CPU of the compute
   A. electronic
   B. mechanic
   C. integrating
   D. processing
   ANSWER: A

3. Microprocessor is the _____ of the computer and it perform all the computational tasks
   A. main
   B. heart
   C. important
   D. simple
   ANSWER: B

4. The purpose of the microprocessor is to control _____
   A. memory
   B. switches
   C. processing
   D. tasks
   ANSWER: A

5. The first digital electronic computer was built in the year_____
   A. 1950
   B. 1960
   C. 1940
   D. 1930
   ANSWER: C

6. In 1960's texas institute invented _____
   A. integrated circuits
   B. microprocessor
   C. vacuum tubes
   D. transistors
   ANSWER: A

7. The intel 8086 microprocessor is a _____ processor
   A. 8 bit
   B. 16 bit
   C. 32 bit
   D. 4 bit
   ANSWER: B

8. The microprocessor can read/write 16 bit data from or to _____
   A. memory
   B. i/o device
   C. processor
   D. register
   ANSWER: A

9. In 8086 microprocessor , the address bus is _____ bit wide
   A. 12 bit
   B. 10 bit
   C. 16 bit
   D. 26 bit
   ANSWER: D

10. The work of EU is _____
    A. encoding
    B. decoding
    C. processing
    D. calculations
    ANSWER: B

11. The 16 bit flag of 8086 microprocessor is responsible to indicate _____
    A. the condition of result of ALU operation
    B. the condition of memory
    C. the result of addition
    D. the result of subtraction
    ANSWER: A

12. The CF is known as _____
    A. carry flag
    B. condition flag
    C. common flag
    D. single flag

ANSWER: A

13. The SF is called as _____
   A. service flag
   B. sign flag
   C. single flag
   D. condition flag
   ANSWER: B

14. The OF is called as _____
   A. overflow flag
   B. overdue flag
   C. one flag
   D. over flag
   ANSWER: A

15. The IF is called as _____
   A. initial flag
   B. indicate flag
   C. interrupt flag
   D. inter flag
   ANSWER: C

16. The register AX is formed by grouping _____
   A. AH & AL
   B. BH & BL
   C. CH & CL
   D. DH & DL
   ANSWER: A

17. The SP is indicated by _____
   A. single pointer
   B. stack pointer
   C. source pointer
   D. destination pointer
   ANSWER: B

18. The BP is indicated by _____
   A. base pointer
   B. binary pointer
   C. bit pointer
   D. digital pointer
   ANSWER: A

19. The SS is called as _____
   A. single stack
   B. stack segment
   C. sequence stack

D. random stack

ANSWER: B

20. The index register are used to hold _____

   A. memory register

   B. offset address

   C. segment memory

   D. offset memory

  ANSWER: A

21. The BIU contains FIFO register of size _____ bytes

   A. 8

   B. 6

   C. 4

   D. 12

  ANSWER: B

22. The BIU prefetches the instruction from memory and store them in _____

   A. queue

   B. register

   C. memory

   D. stack

  ANSWER: A

23. The 1 MB byte of memory can be divided into _____ segment

   A. 1 Kbyte

   B. 64 Kbyte

   C. 33 Kbyte

   D. 34 Kbyte

  ANSWER: B

24. The DS is called as _____

   A. data segment

   B. digital segment

   C. divide segment

   D. decode segme

  ANSWER: A

25. The CS register stores instruction _____ in code segment

   A. stream

   B. path

   C. codes

   D. stream line

  ANSWER: C

26. The IP is _____ bits in length

   A. 8 bits

   B. 4 bits

C. 16 bits
D. 32 bits
ANSWER: C

27. The push source copies a word from source to _____
   A. stack
   B. memory
   C. register
   D. destination
   ANSWER: A

28. LDs copies to consecutive words from memory to register and _____
   A. ES
   B. DS
   C. SS
   D. CS
   ANSWER: B

29. Inc destination increments the content of destination by _____
   A. 1
   B. 2
   C. 30
   D. 41
   ANSWER: A

30. IMUL source is a signed _____
   A. multiplication
   B. addition
   C. subtraction
   D. division
   ANSWER: A

31. _____destination inverts each bit of destination
   A. NOT
   B. NOR
   C. AND
   D. OR
   ANSWER: A

32. The JS is called as _____
   A. jump the signed bit
   B. jump single bit
   C. jump simple bit
   D. jump signal it
   ANSWER: A

33. Instruction providing both segment base and offset address are called _____
   A. below type

B. far type
C. low type
D. high type
ANSWER: B

34. The conditional branch instruction specify _____ for branching
A. conditions
B. instruction
C. address
D. memory
ANSWER: A

35. The microprocessor determines whether the specified condition exists or not by testing the _____
A. carry flag
B. conditional flag
C. common flag
D. sign flag
ANSWER: B

36. The LES copies to words from memory to register and _____
A. DS
B. CS
C. ES
D. DS
ANSWER: C

37. The _____ translates a byte from one code to another code
A. XLAT
B. XCHNG
C. POP
D. PUSH
ANSWER: A

38. The _____ contains an offset instead of actual address
A. SP
B. IP
C. ES
D. SS
ANSWER: B

39. The 8086 fetches instruction one after another from _____ of memory
A. code segment
B. IP
C. ES
D. SS
ANSWER: A

40. The BIU contains FIFO register of size 6 bytes called _____

A. queue
B. stack
C. segment
D. register
ANSWER: A

41. The _____ is required to synchronize the internal operands in the processor CIK Signal
A. UR Signal
B. Vcc
C. AIE
D. Ground
ANSWER: A

42. The pin of minimum mode AD0-AD15 has _____ address
A. 16 bit
B. 20 bit
C. 32 bit
D. 4 bit
ANSWER: B

43. The pin of minimum mode AD0- AD15 has _____ data bus
A. 4 bit
B. 20 bit
C. 16 bit
D. 32 bit
ANSWER: C

44. The address bits are sent out on lines through _____
A. A16-19
B. A0-17
C. D0-D17
D. C0-C17
ANSWER: A

45. _____ is used to write into memory
A. RD
B. WR
C. RD / WR
D. Chk
ANSWER: B

46. The functions of Pins from 24 to 31 depend on the mode in which _____ is operating
A. 8085
B. 8086
C. 80835
D. 80845
ANSWER: B

47. The RD,WR,M/IO is the heart of control for a _____ mode
 A. minimum
 B. maximum
 C. compatibility mode
 D. control mode
 ANSWER: A

48. In a minimum mode there is a _____ on the system bus
 A. single
 B. double
 C. multiple
 D. triple
 ANSWER: A

49. If MN/MX is low the 8086 operates in _____ mode
 A. Minimum
 B. Maximum
 C. both (A) and (B)
 D. medium
 ANSWER: B

50. In max mode, control bus signal So,S1 and S2 are sent out in _____ form
 A. decoded
 B. encoded
 C. shared
 D. un shared
 ANSWER: B

51. The ___ bus controller device decodes the signals to produce the control bus signal
 A. internal
 B. data
 C. external
 D. address
 ANSWER: C

52. A _____ Instruction at the end of interrupt service program takes the execution back to the interrupted program
 A. forward
 B. return
 C. data
 D. line
 ANSWER: B

53. The main concerns of the _____ are to define a flexible set of commands
 A. memory interface
 B. peripheral interface
 C. both (A) and (B)
 D. control interface

ANSWER: A

54. Primary function of memory interfacing is that the _____ should be able to read from and write into register
    A. multiprocessor
    B. microprocessor
    C. dual Processor
    D. coprocessor
    ANSWER: B

55. To perform any operations, the Mp should identify the _____
    A. register
    B. memory
    C. interface
    D. system
    ANSWER: A

56. The Microprocessor places _____ address on the address bus
    A. 4 bit
    B. 8 bit
    C. 16 bit
    D. 32 bit
    ANSWER: C

57. The Microprocessor places 16 bit address on the add lines from that address by _____ register should be selected
    A. address
    B. one
    C. two
    D. three
    ANSWER: B

58. The _____of the memory chip will identify and select the register for the EPROM
    A. internal decoder
    B. external decoder
    C. address decoder
    D. data decoder
    ANSWER: A

59. Microprocessor provides signal like ____ to indicate the read operatio
    A. LOW
    B. MCMW
    C. MCMR
    D. MCMWR
    ANSWER: C

60. To interface memory with the microprocessor, connect register the lines of the address bus must be added to address lines of the _____ chip

A. single
B. memory
C. multiple
D. triple
ANSWER: B

61. The remaining address line of _____ bus is decoded to generate chip select signal
   A. data
   B. address
   C. control bus
   D. both (a) and (b)
   ANSWER: B

62. _____ signal is generated by combining RD and WR signals with IO/M
   A. control
   B. memory
   C. register
   D. system
   ANSWER: A

63. Memory is an integral part of a _____ system
   A. supercomputer
   B. microcomputer
   C. mini computer
   D. mainframe computer
   ANSWER: B

64. _____ has certain signal requirements write into and read from its registers
   A. memory
   B. register
   C. both (a) and (b)
   D. control
   ANSWER: A

65. The memory chips such as 2732 EPROM and _____static R/W memory plays a major role in memory interfacing
   A. 2732 EPROM
   B. 6116
   C. 8085
   D. 8086
   ANSWER: B

66. An _____ is used to fetch one address
   A. internal decoder
   B. external decoder
   C. encoder
   D. register
   ANSWER: A

67. The primary function of the _____ is to accept data from I/P devices
   A. multiprocessor
   B. microprocessor
   C. peripherals
   D. interfaces
   ANSWER: B

68. Designing logic circuits and writing instructions to enable the microprocessor to communicate with peripheral is called _____
   A. interfacing
   B. monitoring
   C. polling
   D. pulling
   ANSWER: A

69. _____ means at the same time, the transmitter and receiver are synchronized with the same clock.
   A. asynchronous
   B. serial data
   C. synchronous
   D. parallel data
   ANSWER: C

70. _____ means at irregular internals
   A. asynchronous
   B. synchronous
   C. data transform
   D. bus transform
   ANSWER: A

71. _____ signal prevent the microprocessor from reading the same data more than one
   A. pipelining
   B. handshaking
   C. controlling
   D. signaling
   ANSWER: B

72. Bits in IRR interrupt are _____
   A. reset
   B. set
   C. stop
   D. start
   ANSWER: B

73. _____ decides the request of interrupt to be serviced
   A. priority resolver
   B. interrupt request register
   C. interrupt mask register

D. control logic

ANSWER: A

74. _____ generate interrupt signal to microprocessor and receive acknowledge

A. priority resolver

B. control logic

C. interrupt request register

D. interrupt register

ANSWER: B

75. The _____ pin is used to select direct command word

A. A0

B. D7-D6

C. A12

D. AD7-AD6

ANSWER: A

76. The _____ is used to connect more microproces

A. peripheral device

B. cascade

C. i/o deviced

D. control unit

ANSWER: B

77. OCW1 is used to set and read _____

A. OCW

B. IMR

C. ICWH

D. EOI

ANSWER: B

78. CS connect the output of _____

A. encoder

B. decoder

C. slave program

D. buffer

ANSWER: B

79. The 8259-A is a _____

A. piority Interrupt Controller

B. priority Resolver

C. interrupt Request Registry

D. control Logic

ANSWER: A

80. The 8259A is used to manage _____ hardware in the system

A. Single

B. Multiple

C. Double

D. none

ANSWER: B

81. _____ is used to transfer data between microprocessor and I/o process

A. 8255A

B. 8279

C. 8254A

D. 8237A

ANSWER: A

82. 8255A contains_____ ports each of 8 bit lines

A. 2

B. 4

C. 5

D. 3

ANSWER: D

83. In 8255A the ____ is controlled by control registers

A. port A

B. port B

C. port C

D. port D

ANSWER: C

84. The read and write operation is done using _____

A. Iow/Ior

B. Iw/Ir

C. Iow

D. Ior

ANSWER: A

85. _____ is used to transfer address connect to address block

A. data bus

B. address bus

C. bus

D. flag

ANSWER: B

86. _____ performs the address decode operation

A. chip select

B. address bus

C. data bus

D. flag

ANSWER: A

87. In 8255A _____ is used for input operation

A. mode 0

B. mode2

C. mode 3

D. mode1

ANSWER: A

88. In 8255A _____ is used for handshaking operation

A. mode 0

B. mode1

C. mode 2

D. mode3

ANSWER: B

89. In 8255 A _____ is used to perform bidirectional operation

A. mode 0

B. mode1

C. mode 2

D. mode3

ANSWER: C

90. Data transfer between the microprocessor for peripheral takes place through _____

A. i/o port

B. input port

C. output port

D. multi port

ANSWER: A

91. The device such as buffer and batches are used as _____.

A. input port

B. output port

C. i/o port

D. multi port

ANSWER: C

92. In 8255A, there are _____ I/o lines

A. 24

B. 12

C. 20

D. 10

ANSWER: A

93. Port A and Port B are used individually as _____ I/o ports

A. 8

B. 16

C. 32

D. 4

ANSWER: A

94. The 8255A is available with _____

A. 20
B. 40
C. 30
D. 10
ANSWER: B

95. 8255A operates with _____ power supply
   A. +5V
   B. -5V
   C. -10V
   D. +10v
   ANSWER: A

96. The pins are _____ data lines and are connected to data bus in system
   A. unidirectional
   B. bidirectional
   C. directional
   D. multidirectional
   ANSWER: B

97. _____ are transferred on the data lines between microprocessor and internal port or control register
   A. data, control and status bites
   B. data and status bits
   C. control and status bites
   D. status bits
   ANSWER: A

98. There are _____ address bus in 8255A
   A. 2
   B. 3
   C. 4
   D. 5
   ANSWER: A

99. The address bus enables the _____ for data transfer.
   A. control register
   B. data bus
   C. address bus
   D. both (b) and (c)
   ANSWER: A

100. The _____ are connected to 2 address bus line in system
   A. address bus
   B. data bus
   C. Pins
   D. control bus
   ANSWER: C

101. The port lines are connected to data lines of the _____
    A. peripheral
    B. microprocessor
    C. address decoder
    D. data decoder
    ANSWER: A

102. The _____ input to 8255A is usually activated by Microprocessor in system
    A. clear
    B. reset
    C. ports
    D. address bus
    ANSWER: B

103. _____ is useful for the generation of accurate time delay
    A. 8254
    B. 8255A
    C. 8237A
    D. 8279
    ANSWER: A

104. _____ is used to refresh D-Ram and regular intervals and provide timing signals
    A. 8255A
    B. 8237A
    C. 8254
    D. 8279
    ANSWER: C

105. The 8254 contains _____ counters
    A. 2-16 bit
    B. 3-16 bit
    C. 2-8 bit.
    D. 3-8 bit
    ANSWER: B

106. The data bus buffer is _____ data line
    A. unidirectional
    B. bidirectional
    C. no direction
    D. multi direction
    ANSWER: B

107. In 8254 there are _____ pins
    A. 20
    B. 24
    C. 30
    D. 40
    ANSWER: B

108. The data lines is used to transfer _____
    A. count, control and status word
    B. data, control and status word
    C. data, count
    D. count status word
    ANSWER: A

109. The _____ input is connected to an output of the address decoder
    A. address bus
    B. data bus
    C. chip select
    D. reset
    ANSWER: C

110. The clock signal of frequency upto _____ is supplied to clock input
    A. 16 MHz
    B. 8 MHz
    C. 32 MHz
    D. 4 MHz
    ANSWER: B

111. The _____ input is used to enable or disable
    A. Clk
    B. out
    C. Reset
    D. gate
    ANSWER: D

112. The _____ generates output way forms on the out and output line
    A. Counter
    B. clock
    C. Gate
    D. out
    ANSWER: A

113. The ____ is constructed for the desired mode and return into control register
    A. control word
    B. clk signal
    C. Gate
    D. reset
    ANSWER: A

114. The internal block of 8237 consists of _____ channels
    A. 2
    B. 3
    C. 4
    D. 5

ANSWER: C

115. The _____ allow data transfer between memory and peripherals
    A. DMA technique
    B. Microprocessor
    C. Register
    D. Decoder
    ANSWER: A

116. The _____ in 8237 operates in either master or in slave mode
    A. microprocessor
    B. register
    C. dma controller
    D. decoder
    ANSWER: C

117. There are _____different types of interface in micro computer system
    A. 3
    B. 4
    C. 5
    D. 2
    ANSWER: D

118. _____ is used in high speed transfer is required
    A. dma technique
    B. serial communication interface
    C. microprocessor
    D. register
    ANSWER: A

119. _____ is used to eliminate clock signal
    A. synchronous
    B. asynchronous
    C. serial
    D. dma
    ANSWER: B

120. Synchronization bit at the beginning of character is called _____
    A. stop bit
    B. simplex
    C. half duplex
    D. start bit
    ANSWER: D

121. Who introduced Pentium family?
    A. intel
    B. wipro
    C. cts

D. samsung

ANSWER: A

122. Pentium pro processor is a _____ generation of device
    A. first
    B. second
    C. third
    D. fourth

ANSWER: B

123. In which year, Pentium pro processor introduced?
    A. 1996
    B. 1998
    C. 1995
    D. 1999

ANSWER: C

124. _____ has been enhanced to provide higher performance for multimedia & communication applications.
    A. Pentium I
    B. Pentium II
    C. Pentium processor with MMX technology
    D. Pentium processor with Celeron technology

ANSWER: C

125. _____ is used in desktop and laptop personal computers
    A. Pentium processor with MMX technology
    B. Pentium Pro Processor
    C. Celeron Processor
    D. Intel Processor

ANSWER: A

126. Expansion of SPGA is _____
    A. Staggered Pin Grid-Array package
    B. Staggered Point Grid-Array package
    C. Staggered Plus Grid-Array package
    D. Staggered per grid-Array package

ANSWER: A

127. Pentium pro processor has _____ die
    A. one
    B. three
    C. two
    D. four

ANSWER: C

128. In Pentium-pro processor, dies are manufactured using intel ___ mm BICMOS process
    A. 0.25

B. 0.35
C. 0.45
D. 0.50
ANSWER: B

129. The circuitry of the Pentium pro processor is equivalent to _____ million transistors
   A. 1.5
   B. 2.5
   C. 3.5
   D. 5.5
ANSWER: D

130. Pentium-pro processor design implements_____ micro architecture
   A. P2
   B. P4
   C. P6
   D. P8
ANSWER: C

131. Micro architecture employs _____ execution
   A. static
   B. dynamic
   C. static and dynamic
   D. none
ANSWER: B

132. _____ is performed to determine the best order of for execution of instructions
   A. system flow analysis
   B. process flow analysis
   C. data flow analysis.
   D. control flow analysis
ANSWER: C

133. Pentium processor with MMX technology includes _____ new instructions and 4 new _____ data types
   A. 50 & 64 bit
   B. 55 & 63 bit
   C. 57 & 64 bit
   D. 51 & 61 bit
ANSWER: A

134. Pentium II processor is a ____generation
   A. first
   B. second
   C. third
   D. fourth
ANSWER: C

135. Pentium II processor was introduced in the year _____.
   A. 1990
   B. 1995
   C. 1998
   D. 1992
   ANSWER: C

136. _____followed Celeron processor and Pentium II Xeon processor
   A. pentium pro processor
   B. pentium ii processor
   C. pentium iii processor
   D. pentium iv processor
   ANSWER: B

137. Pentium II xeon processor offers _____ performance than the std Pentium II processor
   A. lower
   B. higher
   C. medium
   D. none
   ANSWER: B

138. Dual independent bus architecture was first introduced in the _____
   A. pentium pro processor
   B. pentium II processor
   C. pentium III processor
   D. pentium IV processor
   ANSWER: A

139. How many buses provided in Pentium II processor?
   A. one
   B. two
   C. three
   D. four
   ANSWER: B

140. The system bus of both Pentium pro and Pentium II processors carry _____ bytes per clock
   A. 4
   B. 8
   C. 7
   D. 5
   ANSWER: B

141. The maximum speed of Pentium II processor is increased to _____ MHz
   A. 200
   B. 300
   C. 100
   D. 500
   ANSWER: C

142. Backside bus between L2 cache and MPU is _____ speed
   A. higher
   B. lower
   C. medium
   D. Infinite
   ANSWER: A

143. The peak bus bandwidth of backside bus (cache bus) is _____ Mbytes/second
   A. 1000
   B. 1600
   C. 2600
   D. 3400
   ANSWER: B

144. ECC & FRC were first introduced in _____
   A. pentium pro processor
   B. pentium II processor
   C. pentium II xeon processor
   D. pentium III xeon processor
   ANSWER: A

145. Pentium III processor was introduced in _____
   A. 1999
   B. 2000
   C. 2010
   D. 2009
   ANSWER: A

146. Pentium III processor is manufactured using _____ process technology
   A. 0.17
   B. 0.16
   C. 0.18
   D. 0.15
   ANSWER: C

147. In Pentium III processor, the P6 micro architecture is enriched with an additional _____ instructions
   A. 20
   B. 30
   C. 40
   D. 70
   ANSWER: D

148. The 80386 Microprocessor family is a _____ bit microprocessor
   A. 8
   B. 16
   C. 32
   D. 64

ANSWER: C

149. In which year, 80386 microprocessor was introduced?
  A. 1999
  B. 1995
  C. 1985
  D. 1990
ANSWER: C

150. Which family was the sixth member of 8086 family of microprocessors?
  A. 8086
  B. 8085
  C. 80396 DX
  D. 80486 SX
ANSWER: C

151. The 80386DX MPU is the _____ entry in the 80386 family
  A. first
  B. second
  C. third
  D. fourth
ANSWER: A

152. Which device is high-performance member of the 80386 family of MPUs?
  A. 80386SX
  B. 80386DX
  C. 80486SX
  D. 80486DX
ANSWER: B

153. The 80386DX is a full _____ processor
  A. 16 bit
  B. 8 bit
  C. 32 bit
  D. 64 bit
ANSWER: C

154. The 80386DX has both 32 bit internal registers _____ external data bus
  A. 16 bit
  B. 8 bit
  C. 32 bit
  D. 36 bit
ANSWER: C

155. The 80486 family was introduced in the year _____
  A. 1987
  B. 1988
  C. 1989

D. 1990

ANSWER: B

156. _____ maintains real modes protected-mode software compatibility with 80386 architecture

A. 80486

B. 8085

C. 8086

D. 80486 DX

ANSWER: A

157. 80486DX was followed by _____

A. 80486SX

B. 80386SX

C. 80386DX

D. 80486DX

ANSWER: A

158. _____ version did not have a 16-bit external architecture

A. DX

B. SX

C. TX

D. PX

ANSWER: B

159. _____family supports both a math co processor and cache memory

A. 8086

B. 8087

C. 80386

D. 80486

ANSWER: C

160. _____is a co-processor

A. 8086

B. 8087

C. 80386

D. 80486

ANSWER: B

161. The number of hardware chips needed for multiple digit display can be minimized by using the technique called _____

A. interfacing

B. multiplexing

C. demultiplexing

D. multiprocessing

ANSWER: B

162. In multiplexing, the data lines and output ports are time shared by _____

A. Matrix keyboard

B. LCDs
C. LEDs
D. Memory
ANSWER: B

163. I/o ports of programmable devices are limited in current capacity, therefore, additional transistors or ICs called _____
A. LEDs and LCSs
B. interface and multiplexer
C. segment and digit drivers
D. segment drives
ANSWER: C

164. The SN75491 and SN75492 has _____ and _____ Darlington pair transistors in a package respectively
A. 3,8
B. 4,6
C. 2,4
D. 5,10
ANSWER: B

165. _____ is a commonly used input device when more than 8 key are necessary
A. Mouse
B. Joystick
C. Matrix Keyboard
D. Both (a) and (b)
ANSWER: C

166. The _____ reduces the number of connections, thus the number of interfacing device required
A. Mouse
B. Joystick
C. Monitor
D. matrix keyboard
ANSWER: D

167. In scanned multiplexed displays _____ should sink seven or eight times that current
A. Multiplex
B. Demultiplexer
C. Segment
D. Cathode
ANSWER: D

168. The _____ is called segment or digit dri
A. Transistors
B. Cathode
C. Circuit
D. Displays
ANSWER: A

169. The _____ provide the capability of eight I/o ports in interfacing circuit
   A. Encoder
   B. Decoder
   C. Multiplexer
   D. Demultiplexe
   ANSWER: B

170. The output line of interfacing circuit is used in _____
   A. LED scanned display
   B. LCD Scanned display
   C. Keyboard matrix
   D. Display
   ANSWER: A

171. These are _____ common cathode in scanned multiplexed displays
   A. 7
   B. 6
   C. 5
   D. 4
   ANSWER: B

172. There are _____ segment LEDs in scanned multiplexed displays
   A. 5
   B. 4
   C. 6
   D. 7
   ANSWER: D

173. An RS-232 interface is _____
   A. a parallel interface
   B. a serial interface
   C. printer interface
   D. a modem interface
   ANSWER: B

174. Expansion for DTE is _____
   A. data terminal equipment
   B. data trap equipment
   C. data text equipment
   D. data terminal extension
   ANSWER: A

175. Expansion of DCE _____
   A. data circuit terminating equipment
   B. data cycle terminating equipment
   C. data circuit terminating extension
   D. dynamic circuit terminating equipment

ANSWER: A

176. RS-232 is used in _____
   A. common serial port
   B. common signal port
   C. computer serial ports
   D. computer signal port
   ANSWER: C

177. Rs-232 was introduced in _____
   A. 1942
   B. . 1932
   C. 1952
   D. 1962
   ANSWER: D

178. Compared with RS-232, USB is faster and uses_____
   A. medium voltage
   B. higher voltage
   C. lower voltage
   D. None
   ANSWER: C

179. In which year, 8086 was introduced?
   A. 1978
   B. 1979
   C. 1977
   D. 1981
   ANSWER: A

180. In which year, 8088 was announced?
   A. 1979
   B. 1988
   C. 1999
   D. 2000
   ANSWER: A

181. What does the acronym RFID stand for?
   A. remote field identification
   B. radio frequency identification
   C. radio field identification
   D. radio frequency imaging & detection
   ANSWER: B

182. What is a smart card ?
   A. form of ATM card
   B. has more storage capacity than an ATM card
   C. an access card for a security system

D. contains a microprocessor
ANSWER: C

183. Smart Card on a microprocessor is for _____
  A. safety
  B. security
  C. protection
  D. authority
ANSWER: B

184. Smart card is used to provide _____
  A. access
  B. authority
  C. automation
  D. access control
ANSWER: A

185. Another name for smart card _____
  A. ICC
  B. IFC
  C. IRC
  D. IC
ANSWER: A

186. Smart card is made up of _____
  A. silicon
  B. iron
  C. plastic
  D. rubber
ANSWER: C

187. Smart card size is _____
  A. 85.60 x 53.98 mm
  B. 85.70 x53.68 mm
  C. 86.50 x 52.67 mm
  D. 86.40 x51.77 mm
ANSWER: A

188. Smarts cards may have up to _____ kilobytes of RAM, ___ kilobytes of ROM, ___ kilobytes of programmable ROM, and a 16-bit microprocessor
  A. 8 & 346 & 256
  B. 7 & 345 & 255
  C. 6 & 344 & 254
  D. 5 & 343 & 253
ANSWER: A

189. The smart card uses a _____ interface
  A. serial

B. parallel
C. multple
D. single
ANSWER: A

190. The most common smart card application is _____.
  A. credit card
  B. atm card
  C. business card
  D. system card
ANSWER: A

191. Expansion for HMOS technology_____
  A. high level mode oxygen semiconductor
  B. high level metal oxygen semiconductor
  C. high performance medium oxide semiconductor
  D. high performance metal oxide semiconductor
ANSWER: D

192. 8086 and 8088 contains _____ transistors
  A. 29000
  B. 24000
  C. 34000
  D. 54000
ANSWER: A

193. ALE stands for _____
  A. address latch enable
  B. address level enable
  C. address leak enable
  D. address leak extension
ANSWER: A

194. What is DEN?
  A. direct enable
  B. data entered
  C. data enable
  D. data encoding
ANSWER: B

195. Which pin is a programmable peripheral interface?
  A. 8255
  B. 8258
  C. 8254
  D. 8259
ANSWER: A

196. The inside of smart card contains an _____

A. 8085 microprocessor
B. 8086 microprocessor
C. 8088 microprocessor
D. embedded microprocessor
ANSWER: D

197. RFID technology is a _____
   A. automatic identification technology
   B. computer tech
   C. information tech
   D. system tech
ANSWER: A

198. The information stored in RFID is _____
   A. character
   B. number
   C. ascii
   D. pneumonic
ANSWER: C

199. In RFID, the productivity enhancement is _____ time
   A. five
   B. ten
   C. four
   D. nine
ANSWER: B

200. RFID chip inside the tag is _____
   A. read only
   B. write only
   C. read-write
   D. none
ANSWER: A

201. Which interrupt has the highest priority?
   A. INTR
   B. TRAP
   C. RST6.5
   D. RST6.6
ANSWER: C

202. In 8085 name the 16 bit registers?
   A. stack pointer
   B. program counter
   C. a & b
   D. stack register
ANSWER: C

203. Which of the following is hardware interrupts?
  A. RST5.5, RST6.5, RST7.5 .
  B. INTR, TRAP . .
  C. a & b.
  D. .INTR
  ANSWER: C

204. What is the RST for the TRAP?
  A. RST5.5
  B. RST4.5
  C. RST4
  D. RST3
  ANSWER: B

205. What are level Triggering interrupts?
  A. INTR&TRAP.
  B. RST6.5&RST5.5.
  C. RST7.5&RST6.5.
  D. RST2.5 & RST6.2.
  ANSWER: B

206. Which interrupt is not level sensitive in 8085?
  A. RST6.5 is a raising edge-trigging interrupt.
  B. RST7.5 is a raising edge-trigging interrupt.
  C. RST5.5.
  D. RST4.5.
  ANSWER: B

207. What are software interrupts?
  A. RST 0-7
  B. RST 5.5 - 7.5
  C. INTR, TRAP
  D. RST 4.4 - 6.4
  ANSWER: A

208. Which stack is used in 8085?
  A. FIFO.
  B. LIFO.
  C. FILO
  D. LILO.
  ANSWER: B

209. Why 8085 processor is called an 8 bit processor?
  A. because 8085 processor has 8 bit alu.
  B. because 8085 processor has 8 bit data bus.
  C. because 8085 processor has 16 bit data bus.
  D. because 8085 processor has 16 bit address bus.
  ANSWER: A

210. What is SIM?
   A. Select Interrupt Mask .
   B. Sorting Interrupt Mask.
   C. Set Interrupt Mask
   D. Set Integer Mask
   ANSWER: C

211. RIM is used to check whether, the _____.
   A. write operation is done or not .
   B. interrupt is Masked or not .
   C. interrupt is Masked.
   D. interrupt is not Masked.
   ANSWER: B

212. What is meant by maskable interrupts?
   A. an interrupt which can never be turned off.
   B. an interrupt that can be turned off by the programmer.
   C. an interrupt which can never be turned on.
   D. an interrupt which can never be turned on or off.
   ANSWER: B

213. In 8086, Example for Non maskable interrupts are _____.
   A. trap.
   B. rst6.5.
   C. intr.
   D. rst6.6.
   ANSWER: A

214. What does microprocessor speed depends on?
   A. clock.
   B. data bus width.
   C. address bus width.
   D. signal bus.
   ANSWER: C

215. _____ can be used as stack .
   A. ROM.
   B. RAM.
   C. EPROM
   D. PROM
   ANSWER: B

216. Which processor structure is pipelined?
   A. all x80 processors.
   B. all x85 processors.
   C. all x86 processors.
   D. all x87 processors.

ANSWER: C

217. Address line for RST3 is?
   A. 0020H.
   B. 0028H.
   C. 0018H.
   D. 0019H
   ANSWER: C

218. In 8086 the overflow flag is set when _____.
   A. the sum is more than 16 bits.
   B. signed numbers go out of their range after an arithmetic operation.
   C. carry and sign flags are set.
   D. subtraction
   ANSWER: B

219. The advantage of memory mapped I/O over I/O mapped I/O is _____
   A. faster.
   B. many instructions supporting memory mapped I/O.
   C. require a bigger address decoder.
   D. all the above
   ANSWER: D

220. BHE of 8086 microprocessor signal is used to interface the _____.
   A. even bank memory.
   B. odd bank memory.
   C. i/o.
   D. direct memory access
   ANSWER: B

221. In 8086 microprocessor the following has the highest priority among all type interrupts?
   A. NMI.
   B. DIV 0.
   C. TYPE 255.
   D. OVER FLOW
   ANSWER: A

222. In 8086 microprocessor one of the following statements is not true?
   A. coprocessor is interfaced in max mode.
   B. coprocessor is interfaced in min mode.
   C. i/o can be interfaced in max / min mode.
   D. supports pipelining
   ANSWER: B

223. 8088 microprocessor differs with 8086 microprocessor in _____.
   A. data width on the output.
   B. address capability.
   C. support of coprocessor.

D. support of MAX / MIN mode

ANSWER: A

224. Address line for TRAP is?

A. 0023H.

B. 0024H.

C. 0033H.

D. 0099H.

ANSWER: B

225. Access time is faster for _____.

A. ROM.

B. SRAM.

C. DRAM.

D. ERAM

ANSWER: B

226. In 8279 Strobed input mode, the control line goes low. The data on return lines is strobed in the

_____.

A. FIFO byte by byte.

B. FILO byte by byte.

C. LIFO byte by byte.

D. LILO byte by byte.

ANSWER: A

227. _____ bit in ICW1 indicates whether the 8259A is cascade mode or not?

A. LTIM=0.

B. LTIM=1.

C. SNGL=0.

D. SNGL=1.

ANSWER: C

228. In 8255, under the I/O mode of operation we have _____ modes. Which mode will have the following features?

A. A 5 bit control port is available.

B. Three I/O lines are available at Port C.

C. 3, mode2.

D. 2, mode 2.

ANSWER: B

229. In ADC 0808 if _____ pin high enables output

A. EOC.

B. I/P0-I/P7.

C. SOC.

D. OE.

ANSWER: D

230. In 8279, a scanned sensor matrix mode, if a sensor changes its state, the _____ line goes

_____ to interrupt the CPU
   A. CS, high.
   B. A0, high.
   C. IRQ, high.
   D. STB, high
   ANSWER: C

231. In 8279 Status Word, data is read when _____ pins are low, and write to the display RAM with
_____ are low.
   A. A0, CS, RD & A0, WR, CS.
   B. CS, WR, A0 & A0, CS, RD.
   C. A0, RD & WR, CS.
   D. CS, RD & A0, CS.
   ANSWER: A

232. In 8279, the keyboard entries are de bounced and stored in an _____, that is further accessed by
the CPU to read the key codes.
   A. 8-bit FIFO.
   B. 8-byte FIFO.
   C. 16 byte FIFO.
   D. 16 bit FIFO
   ANSWER: B

233. The 8279 normally provides a maximum of _____ seven segment display interface with CPU.
   A. 8.
   B. 16.
   C. 32.
   D. 18.
   ANSWER: B

234. For the most Static RAM the write pulse width should be at least
   A. 10ns.
   B. 60ns.
   C. 300ns.
   D. 1μs.
   ANSWER: B

235. BURST refresh in DRAM is also called as _____.
   A. concentrated refresh.
   B. distributed refresh.
   C. hidden refresh.
   D. signal refresh
   ANSWER: A

236. For the most Static RAM the maximum access time is about _____.
   A. 1ns.
   B. 10ns.
   C. 100ns.

D. 1μs

ANSWER: C

237. Which of the following statements on DRAM are correct? Page mode read operation is faster than RAS read. RAS input remains active during column address strobe. The row and column addresses are strobed into the internal buffers using RAS and CAS inputs respectively

A. i & iii.

B. i & ii.

C. all.

D. iii.

ANSWER: C

238. 8086 microprocessor is interfaced to 8253 a programmable interval timer. The maximum number by which the clock frequency on one of the timers is divided by _____.

A. 2^16

B. 2^8

C. 2^10

D. 2^20

ANSWER: A

239. 8086 is interfaced to two 8259s (Programmable interrupt controllers). If 8259s are in master slave configuration the number of interrupts available to the 8086 microprocessor is _____.

A. 8.

B. 16.

C. 15.

D. 64

ANSWER: D

240. The First Microprocessor was_____.

A. Intel 4004

B. 8080

C. 8085

D. 4008

ANSWER: A

241. 8085 was introduced in _____.

A. 1971

B. 1976

C. 1972

D. 1978

ANSWER: B

242. In 1978 Intel introduced the 16 bit Microprocessor 8086 now called as_____.

A. M6 800

B. APX 80

C. Zylog z8000

D. Intel 8086

ANSWER: B

243. Which is a 8 bit Microprocessor ?
   A. Intel 4040
   B. Pentium-I
   C. 8088
   D. Motorala MC-6801
   ANSWER: D

244. Pentium-I, Pentium-II, Pentium-III and Pentium-IV are recently introduced microprocessor by_____.
   A. Motorala.
   B. Intel.
   C. Stephen Mors.
   D. HCL.
   ANSWER: B

245. The address bus flow in _____.
   A. bidirection.
   B. unidirection.
   C. mulidirection.
   D. circular.
   ANSWER: B

246. Status register is also called as _____.
   A. accumulator.
   B. stack.
   C. counter.
   D. flags
   ANSWER: D

247. The 8085 is based in a _____ pin DIP
   A. 40.
   B. 45.
   C. 20.
   D. 35
   ANSWER: A

248. The 8085 Microprocessor uses_____ V power suppl
   A. .+5V.
   B. -5V.
   C. +12V.
   D. -12V
   ANSWER: A

249. The address / data bus in 8085 is _____.
   A. multiplexed.
   B. demultiplexed.
   C. decoded.

D. encoded

ANSWER: A

250. The First electronic computer was completed in _____.

   A. 1946.

   B. .1938.

   C. 1941.

   D. .1950

ANSWER: A