# MGU-BCA-205- Second Sem- Core VI- Fundamentals of Digital SystemsMCQ's 

## Unit-1 Number Systems

1. What does a decimal number represents?
A. Quality
B. Quantity
C. Position
D. None of the above
2. Why the decimal number system is also called as positional number system?
A. Since the values of the numbers are decided by multiplying the values.
B. Since the values of the numbers are decided by the weight of the values.
C. Since the values of the numbers are decided by adding the values.
D. Since the values of the numbers are decided by the position of the values.
3. In binary number system a digit ranges from $\qquad$ .
A. 0 to 9
B. 0 to 1
C. 0 to 15
D. 0 to 7
4. How can you represent a decimal point?
A. By a series of coefficients.
B. By weight decided by its position.
C. By location as well as base
D. None of the above
5. A digit in base R will have a range from $\qquad$ .
A. 1 to $\mathrm{R}-1$
B. 0 to $\mathrm{R}-1$
C. 1 to $\mathrm{R}+1$
D. 0 to $\mathrm{R}+1$
6. Conversion from any base to decimal base is done by $\qquad$ each digit by its corresponding weight and then $\qquad$ all the individual products to get the equivalent decimal value.
A. Multiplying, Adding
B. Adding, Multiplying
C. Dividing, Adding
D. Adding, Subtracting
7. Which method is used to convert a number from an octal base to decimal base?
A. Direct conversion method
B. Decimal equivalent method
C. Octal equivalent method
D. Positional notation method
8. In which conversion the product of number 16 raised by the location and then add all the products to get the final decimal value?
A. Octal to decimal
B. Binary to Decimal
C. Hexadecimal to decimal
D. None of the above
9. Binary numbers can be converted into equivalent octal numbers by making groups of three bits $\qquad$ .
A. Starting from the MSB
B. Starting from the LSB
C. Ending at the MSB
D. Ending at the LSB

10 . What is the octal equivalent of 58 , 3-bit binary number?
A. $010_{2}$
B. $110_{2}$
C. $000_{2}$
D. $101_{2}$
11. In direct conversion from binary to hexadecimal, if the last group does not have 4bits, then it is padded with $\qquad$ to make it four bits.
A. Zeros
B. Ones
C. Two zeros and two ones
D. One zero and three ones
12. What is the hex equivalent of $9_{16,}$ a 4 -bit binary number?
A. $1111_{2}$
B. $1001_{2}$
C. $0110_{2}$
D. $1100_{2}$
13. The sign information has to be encoded along with the $\qquad$ to represent the integers completely.
A. No. of bits
B. Position
C. Magnitude
D. Weight
14. Which one is the possible technique for representing signed integers?
A. Signed Magnitude Representation
B. Diminished Radix-Complement Representation
C. Radix-Complement Representation
D. All of the above
15. What is used to represent the signed magnitude?
A. MSB
B. LSB
C. Both
D. None of the above
16. What is the corresponding hex number of the signed magnitude -127 ?
A. $(7 \mathrm{~F})_{16}$
B. $(\mathrm{FF})_{16}$
C. $(00)_{16}$
D. $(80)_{16}$
17. What are the two ways of representing the 0 with signed magnitude representation?
A. -0 and -0
B. +0 and +0
C. -0 and +0
D. None of the above
18. $(\mathrm{FA})_{16}$ is the $\qquad$ one's complement representation of -5 .
A. 4-bit
B. 8 -bit
C. 16-bit
D. 2-bit
19. 2's complement is used to represent signed integers, especially integers.
A. Negative
B. Positive
C. Both A and B
D. None of the above
20. In $\qquad$ , to encode a negative number, first the binary representation of its magnitude is taken, complement each bit and then add 1.
A. Signed integer representation
B. 1's complement representation
C. 2's complement representation
D. Radix complement representation
21. Which one of the following is the type of complement for each base R system?
A. Diminished radix-complement representation [( $\mathrm{R}-1$ )'s complement]
B. Radix- complement representation [R's complement]
C. 1's and 2's complement representation
D. Both A and B
22. For subtraction of binary number, subtract the $\qquad$ .
A. Minuend from the subtrahend digit
B. Subtrahend digit from the minuend
C. MSB from the LSB
D. None of the above
23. Which of the following condition is true for determining overflow condition in 2 's complement?
A. When adding two positive numbers gives a negative result or when two negatives give a positive result.
B. If sign bit (MSB) of result and sign bit of two operands are of different signs.
C. The ' 1 ' in the MSB position indicates a negative number after adding two positive numbers.
D. All of the above
24. What does the leftmost bit represents, according to the IEEE standards?
A. Sign of the number
B. Position of the number
C. Weight of the number
D. None of the above
25. Floating-point numbers are those numbers, which include $\qquad$ .
A. Decimals
B. Fractional parts
C. Integer values
D. All of the above
26. The binary representation of 0.875 is 00111111011000000000000000000000 in presentation.
A. 128- bit
B. Excess 127
C. 32-bit
D. 16 -bit
27. 1000001 represents as $(65)_{10}$ in which code?
A. ASCII code
B. Straight binary code
C. Gray code
D. BCD code
28. Binary Coded Decimal or BCD is also known as $\qquad$ .
A. 2841
B. 4821
C. 4281
D. 8421
29. In straight binary code, N -bits or N binary digits can represent $\qquad$ different values.
A. $2^{\mathrm{N}}$
B. $2^{\mathrm{N}+1}$
C. $2^{\mathrm{N}-1}$
D. $2^{\mathrm{N}}-1$
30. What is the decimal representation of decimal number 5 ?
A. 0000
B. 1001
C. 0011
D. 0101
31. Which of the following code is also known as reflected code?
A. Excess- 3 codes
B. Gray code
C. Straight binary code
D. Error code
32. EXOR is the $\qquad$ of the binary number.
A. MSB to the next bit
B. LSB to the next bit
C. MSB of the previous bit
D. LSB of the previous bit
33. ASCII code is required for representing more than $\qquad$ characters.
A. 16
B. 8
C. 64
D. 32
34. Why the 8-bit (MSB) is added in EBCDIC?
A. For carriage return
B. For making the total number of 1's odd
C. For line feed
D. For parity
35. What is the 8 -bit EBCDIC representation of alphabet M?
A. 1100100
B. 11001001
C. 11010100
D. 010001
36. What will be the result in BCD form if two binary numbers 599 and 984 are added?
A. 1583
B. 8513
C. 8421
D. None of the above
37. Which of the following is not correct regarding EBCDIC?
A. It is used to represent more than 64 characters.
B. It is a 7-bit code.
C. A maximum of 128 different characters can be represented by this code.
D. None of the above
38. The MSB of $\qquad$ is same as the MSB of the corresponding Gray code.
A. Alphanumeric code
B. Excess-3 code
C. Binary code
D. Gray code
39. How can you represent $(08)_{10}$ in BCD ?
A. 00001000
B. 00100011
C. 100100100001
D. 10010010
40. In N-bits, you can represent the signed integers ranging from $\qquad$ .
A. $2^{(\mathrm{N}-1)}$ to $2^{(\mathrm{N}+1)}$
B. $-2^{(\mathrm{N}-1)}$ to $2^{(\mathrm{N}-1)}-1$
C. $2^{(\mathrm{N}+1)}$ to $2^{(\mathrm{N}-1)}+1$
D. $2^{(\mathbb{N})}$ to $2^{(\mathrm{N}+1)}$
41. How -5 is represented in hex format in 2 's complement in 8-bits?
A. $(\mathrm{FB})_{16}$
B. $(7 \mathrm{~F})_{16}$
C. $(\mathrm{FF})_{16}$
D. $(\mathrm{FA})_{16}$
42. To convert $\qquad$ , write the number to be converted, placing each digit under the proper position.
A. Any base to decimal base
B. Hexadecimal number to decimal base
C. Decimal base to octal base
D. Octal base to decimal base
43. In which type of conversion, binary numbers can be converted into equivalent octal numbers by making groups of three bits starting from the LSB, moving towards the MSB of the number and then replacing each group of three bits by its octal representation.
A. Conversion of decimal fraction to any base
B. Conversion from decimal base to any base
C. Direct conversion from binary to hexadecimal
D. Direct conversion from binary to octal
44. What is the 9 's complement of $(0.3267)_{10}$ ?
A. 47.479
B. 0.6352
C. 0.6732
D. 1.4563
45. In subtraction of binary numbers, if the subtrahend digit is greater than the minuend, then borrow from a $\qquad$ significant bit.
A. Lower
B. Higher
C. First
D. None of the above
46. Which of the following cases leads to the overflow condition in addition using 2 's complement?
A. Addition of two positive numbers, which results in sum $\square \geq 2^{\mathrm{n}-1}$
B. Addition of two positive numbers, which results in sum $<2^{\mathrm{n}-1}$
C. Addition of two negative numbers, $\mid$ suml $\square \leq \square 2^{\mathrm{n}-1}$
D. Addition of two negative numbers, $\mid$ suml $>2^{\mathrm{n}-1}$
47. Which of the following case is known as end-around carry addition?
A. Addition of two positive numbers, which results in sum $\square \geq 2^{\mathrm{n}-1}$
B. Addition of two positive numbers, which results in sum $<2^{\mathrm{n}-1}$
C. Addition of positive and negative numbers (-ve number largest magnitude).
D. Addition of positive and negative numbers (+ve number largest magnitude).
48. In, subtraction of positive numbers using radix complement representation ( $\mathrm{M}-\mathrm{N}$ ), If number of digits are not same in M and N how can you make them equal?
A. By appending 1 at the end
B. By appending 1 at the beginning
C. By appending 0 at the beginning
D. By appending 0 at the end
49. Which sign bit is used for representing the positive sign in floating point representation?
A. 0
B. 1
C. Either A or B
D. None of the above
50. How can you represent $=$ in 8 -bit EBCDIC representation?
A. 01111111
B. 01111110
C. 01011100
D. 01101011

## Unit 2- Boolean Algebra and Gate Networks

1. Logic High at the output is treated as gate $\qquad$
(A) On
(B) Off
(C) 0
(D) None of the above
2. In digital electronics, the ' ON ' state is often represented by 1
(A) 0
(B) 1
(C) 2
(D) 3
3. The basic logic gates are NOT, AND, $\qquad$
$\qquad$ and
$\qquad$ .
(A) OR
(B) XOR
(C) XNOR
(D) All of the above
4. The output of the NOT gate is always the $\qquad$ of the input.
(A) Same
(B) Negation
(C) Opposite
(D) Both (B) and (C)
5. A basic AND gate consists of $\qquad$ inputs and an output.
(A) One
(B) Zero
(C) Two
(D) Ten
6. In the AND gate, the output is 'High' or gate is 'On' only if both the inputs are
$\qquad$
(A) Fluctuating
(B) Low
(C) Medium
(D) High
7. Symbol: $\mathrm{F}=\mathrm{A} . \mathrm{B}$, where '. ' implies $\qquad$ operation.
(A) OR
(B) AND
(C) XOR
(D) NOR
8. A basic OR gate is a two input, $\qquad$ output gate.
(A) Two
(B) Infinity
(C) Single
(D) Zero
9. The OR gate output is 0 only when both the inputs are $\qquad$ .
(A) Minus
(B) 2
(C) 1
(D) 0
10. Symbol: F = A + B, where ' + ' implies $\qquad$ operation.
(A) OR
(B) AND
(C) NAND
(D) XOR
11. A gate related to the OR gate is the $\qquad$ or $\qquad$ _.
(A) NOR
(B) XOR Gate
(C) Exclusive OR Gate
(D) Both (B) and (C)
12. The XOR output is 1 if the inputs are $\qquad$ .
(A) Different
(B) Same
(C) Finite
(D) Infinite
13. Symbol: $\mathrm{F}=\mathrm{A} \oplus \mathrm{B}$, where ' $\oplus$ ' implies $\qquad$ operation.
(A) OR
(B) XOR
(C) NOR
(D) NAND
14. In addition to the NOT, AND, OR and XOR gates $\qquad$ more common gates are available.
(A) Four
(B) One
(C) Two
(D) Three
15. For multi-input AND and NAND gates, the unused input pin should not be left
$\qquad$ .
(A) ON
(B) Connected
(C) Unconnected.
(D) None of the above
16. For multi-input XNOR gate, the output is Logic High when the total number of Logic High in the inputs signals is $\qquad$ .
(A) Infinity
(B) Zero
(C) Odd
(D) Even
17. When one of the inputs of two-input a XOR gate is Logic High, the output will be $\qquad$ of the other input.
(A) NOR
(B) NOT
(C) XOR
(D) None of the above
18. When one of the inputs of two-input XOR gates is Logic Low, the output will be the $\qquad$ as the other input.
(A) Same
(B) Different
(C) Common
(D) All the above
19. When a logic circuit diagram is given, you can analyse the circuit to obtain the
$\qquad$ _.
(A) Result
(B) Input
(C) Logic Expression
(D) None of the above
20. Boolean algebra is named after $\qquad$ , who used it to study human logical reasoning.
(A) Anderson, Mary
(B) Acharya Kanad
(C) Dickson, Earle
(D) George Boole
21. For every $x$, $y$ in $B$,
$n x+y=y+x$
n $x$. $y=y . x$
(A) Commutative Law
(B) Complement
(C) Closure
(D) None of the above
22. Every valid Boolean expression (equality) remains valid if the operators and identity elements are interchanged.
(A) Distributive Law
(B) Complement
(C) Duality Principle
(D) None of the above
23. For every $x$, y in B,
$n \mathrm{x}+\mathrm{y}$
n x. y
(A) Closure
(B) Hand-held
(C) Commutative Law
(D) Identities
24. A $\qquad$ is a table, which consists of every possible combination of inputs and its corresponding outputs.
(A) Last table
(B) Truth Table
(C) K- Map
(D) None of the above
25. In the truth table formation, inputs are taken as $\mathrm{A}_{1} \mathrm{~A}_{0}$ for A input and
$\qquad$ for B input.
(A) $\mathrm{A}_{1} \mathrm{~B}_{1}$
(B) $A_{0} B_{1}$
(C) $\mathrm{B}_{0} \mathrm{~B}_{1}$
(D) $\mathrm{B}_{1} \mathrm{~B}_{0}$
26. The Boolean expression for the output $F_{1}$ will be $F_{1}=x . y . z^{\prime}$. This is
$\qquad$ form.
(A)Product-of-Sum
(B) Sum-of-Products
(C) Straight
(D) None of the above
27. For a function $F$, the complement of this function $F^{\prime}$ is obtained by interchanging 1 with
(A) 0
(B) 100
(C) 110
(D) One-Fourth
28. A variable on its own or in its complemented form is known as
a $\qquad$ _.
(A) Product Term
(B) Literal
(C) Sum Term
(D) All of the above
29. It is a single literal or a logical product (AND) of several literals.
(A) SOP
(B) POS
(C) Literal
(D) Product Term
30. It is a sum term or a logical product (AND) of several sum terms.
(A) SOP
(B) Minterm
(C) POS
(D) Either (A) or (B)
31. Maxterm is the sum of $\qquad$ of the corresponding Minterm with its literal complemented.
(A) Terms
(B) Words
(C) Numbers
(D) None of the above
32. Canonical form is a unique way of representing $\qquad$ .
(A) SOP
(B) Minterm
(C) Boolean Expressions
(D) A page
33. Maxterms of a function are the terms for which the result is $\qquad$ .
(A) Numerical
(B) Words
(C) Characters
(D) 0
34. A Karnaugh map (K-map) is an abstract form of $\qquad$ diagram, organized as a matrix of squares,
(A) Venn Diagram
(B) Cycle Diagram
(C) Block diagram
(D) Triangular Diagram
35. There are $\qquad$ Minterms for 3 variables ( $\mathrm{a}, \mathrm{b}, \mathrm{c}$ ).
(A) 0
(B) 2
(C) 8
(D) None of the above
36. There are $\qquad$ cells in a 4 -variable K-map.
(A) 12
(B) 16
(C) 18
(D) All of the above
37. The K-map based Boolean reduction is based on the following Unifying Theorem:
$\mathrm{A}+\mathrm{A}^{\prime}=1$
(A) Impact
(B) Non Impact
(C) Force
(D) None of the above
38. Each product term of a group, $w^{\prime} \cdot x \cdot y^{\prime}$ and w.y, represents the $\qquad$ in that group.
(A) Input
(B) POS
(C) Sum-of-Minterms
(D) Both (A) and (B)
39. The prime implicant, which has at least one element that is not present in any other implicant, is known as $\qquad$ —.
(A) Essential Prime Implicant
(B) Implicant
(C) Complement
(D) All of the Above
40. Product-of-Sums expressions can be implemented using
(A) 2-level OR-AND logic circuits
(B) 2-level NOR logic circuits
(C) 2-level XOR logic circuits
(D) Both (A) and (B)
41. Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given $\qquad$ .
(A) Function
(B) Value
(C) Set
(D) None of the above
42. How to find the Simplest SOP expression?
(A) Circle all odd implicants on the K-map.
(B) Identify and delete all essential prime implicants for the cover.
(C) Select a maximum subset of the remaining prime implicants to complete the cover, that is, to cover those Minterms not covered by the essential prime implicants.
(D) None of the above
43. Don't care conditions can be used for simplifying Boolean expressions in $\qquad$ .
(A) Examples
(B) Terms
(C) K-maps
(D) Either (A) or (B)
44. It should be kept in mind that don't care terms should be used along with the terms that are present in $\qquad$ _.
(A) Minterms
(B) Maxterm
(C) K-Map
(D) None of the above
45. $\qquad$ expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits.
(A)POS
(B) Literals
(C) (SOP)
(D) All of the above
46. Using the transformation method discussed, you can realize any POS realization of OR-AND with only.
(A) XOR
(B) NAND
(C) AND
(D) NOR
47. There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and $\qquad$ operations.
(A) XNOR
(B) XOR
(C) NOR
(D) All of the above
48. These logic gates are widely used in $\qquad$ design, and therefore are available in IC form.
(A) Circuit
(B) Digital
(C) Analog
(D) Block
49. In case of $X O R / X N O R$ simplification, you have to look for the following
(A) Diagonal Adjacencies
(B) Offset Adjacencies
(C) Straight Adjacencies
(D) Both (A) and (B)
50. Entries known as $\qquad$ mapping.
(A) Diagonal
(B) Straight
(C) K
(D) None of the above

## Unit 3- Sequential and Combinational Logic Structure

1. It is a simple combinational digital circuit built from logic gates
(A) Full Adder
(B) Half Adder
(C) Null Adder
(D) None of the above
2. It is used to subtract two inputs having more than one bit
(A) Full Subtractor Circuit
(B) Half Subtractor
(C) Multiplexer
(D) Counter
3. It is a circuit, which subtracts two inputs each of one bit
(A) Full Subtractor
(B) Full Adder
(C) Half Subtractor
(D) All of the above
4. A code converter circuit converts the code of one form to another form
(A) Encoder
(B) Code Converter
(C) Decoder
(D) Both (B) and (C)
5. It is the converse of decoding and contains $2^{n}$ (or fewer) input lines and $n$ output lines
(A) Subtractor
(B) Decoder
(C) Multiplexer
(D) Encoder
6. It directs data from input to a selected output line
(A) Demultiplexer
(B) Multiplexer
(C) Coder
(D) Both (A) and (B)
7. It is a very useful combinational circuit used in communication systems
(A) Parity bit Checker
(B) Parity bit Generator
(C) Parity bit
(D) Both (A) and (B)
8. This converter deals with converting binary code to gray code
(A) Binary to Gray Code Converter
(B) Gray to Binary Code Converter
(C) Binary Code Converter
(D) Gray Code Converter
9. It compares two n-bit values to determine whether one of them is greater or if they are equal
(A) Calculator
(B) Multiplexer
(C) Comparator
(D) None of the above
10. It is a circuit, which has a number of input lines and selection lines with one output line
(A) Sequential Circuit
(B) Multiplexer
(C) Counter
(D) All of the above
11. It is a circuit, which can remember values for a long time or change values when required
(A) Ripple
(B) Counter
(C) Circuit
(D) Memory Element
12. It is a sequential circuit that cycles through a sequence of states
(A) Multiplexer
(B) Demultiplexer
(C) Counter
(D) Ripple
13. It is a counter where the flip-flops do not change states at exactly the same time, as they do not have a common clock pulse.
(A) Asynchronous Ripple Counter
(B) Synchronous Ripple Counter
(C) Counter
(D) All of the above
14. It is a bi-directional counter capable of counting in either of the direction depending on the control signal
(A) Up Synchronous Counter
(B) Down Synchronous Counter
(C) Synchronous Counter
(D) Both (A) and (B)
15. In this logic, output depends not only on the current inputs but also on the past input values. It needs some type of memory to remember the past input values
(A)Logical Circuit
(B) Connected Circuit
(C) Sequential Circuit
(D) Parallel Circuit
16. It consists of two-level AND-OR circuits on a single chip
(A) PLA
(B) PAL
(C) ALP
(D) None of the above
17. It is a programmable array of logic gateson a single chip in AND-OR configuration
(A) PLA
(B) PAL
(C) XOR APL
(D) All of the above
18. In a combinational circuit, each output depends entirely on the $\qquad$ inputs to the circuit.
(A) Same
(B) Different
(C) Common
(D) Immediate
19. In $\qquad$ circuit, the output depends on both the present and the past inputs.
(A) Parallel
(B) Sequential
(C) Combinational
(D) None of the above
20. The steps required for the analysis of combinational circuits are
(A)Label the inputs and outputs.
(B)Obtain the functions of intermediate points and the outputs.
(C)Draw the truth table
(D) All of the above
21. IC chips based on packaging density are
(A) Small-Scale Integration (SSI): Up to 12 gates.
(B) Medium-Scale Integration (MSI): 12-99 gates.
(C) Small- Scale Integration (SSI): Up to 14 gates
(D) Both (A) and (B)
22. While designing a digital system, the main objectives are
(A) Low cost
(B) Less number of gates
(C) Increased Speed
(D) All of the above
23. There are two types of parity,
(A) Even
(B) Odd
(C) First
(D) Both (A) and (B)
24. Using a $\qquad$ , and by interchanging input and output entries, you can design a Gray to binary code converter.
(A) Last table
(B) Truth Table
(C) K- Map
(D) None of the above
25. Circuits that are more complex can be built using the $\qquad$ method.
(A) First- level
(B) Digital Level
(C) Block Level
(D) None of the above
26. BCD-to-Excess-3 Code Conversion is a example of a $\qquad$ .
(A) 4-bit Parallel Adder
(B) Sum-of-Products
(C) 2- bit Parallel Adder
(D) None of the above
27. $\qquad$ can be performed through addition using the 2's
complement method.
(A) Division
(B) Multiplication
(C) Addition
(D) Subtraction
28. The four common and useful MSI circuits are
(A) Decoder
(B) Demultiplexer
(C) Encoder
(D) All of the above
29. Codes are frequently used to represent $\qquad$ -
(A) Entities
(B) POS
(C) Literal
(D) Product Term
30. Decoders often come with an enable signal, so that the device is only activated when the enable E equals to $\qquad$ .
(A) 2
(B) 1
(C) 3
(D) Either (A) or (B)
31. When more than one input can be active, the priority $\qquad$ must be used.
(A) Terms
(B) Words
(C) Encoder
(D) None of the above
32. The Boolean expression for the multiplexer can be derived by the inspection method.
(A) $6 \times 1$
(B) $3 \times 1$
(C) $5 \times 1$
(D) $4 \times 1$
33. $\qquad$ multiplexers can be constructed from smaller ones.
(A) Small
(B) Larger
(C) Dimultiplexers
(D) All of the above
34. A $\qquad$ is a circuit, which can remember values for a long time or change values when required.
(A)Logical Circuit
(B) Digital Circuit
(C) Memory Element
(D) Complex Circuit
35. A $\qquad$ circuit is not suitable in the synchronous circuit design because of its transparency nature.
(A) Latch
(B) Parallel
(C) Diagonal Circuit
(D) None of the above
36. There are $\qquad$ basic types of flip-flop based on clock trigger.
(A) 2
(B) 6
(C) 8
(D) 4
37. The characteristic equation of any flip-flop describes the
$\qquad$ of the next state in terms of the present state and inputs.
(A) Impact
(B) Behavior
(C) Path
(D) None of the above
38. The normal data inputs to a flip-flop ( $\mathrm{D}, \mathrm{S}$ and $\mathrm{R}, \mathrm{J}$ and $\mathrm{K}, \mathrm{T}$ ) are referred to as
$\qquad$ inputs
(A) Sequential
(B) Asynchronous
(C) Synchronous
(D) Both (A) and (B)
39. Asynchronous inputs, just like synchronous inputs, can be engineered to be
$\qquad$
(A) Active-Medium
(B) Active-Low
(C) Active-High
(D) Both (B) and (C)
40. $\qquad$ and Clear should not be 0 at the same time; otherwise, both the outputs will be 1 , which is known as invalid state.
(A) Preset
(B) Post set
(C) Fixed
(D) Both (A) and (B)
41. Which table indicates the input conditions of the flip-flops necessary to cause all possible next state transitions of a flip-flop?
(A) T characteristic
(B) Truth
(C) Flip- flop excitation
(D) Excitation
42. When a circuit is self- correcting?
(A) If there are $\mathrm{N}-1$ cycles among its unused states
(B) If there are $\mathrm{N}-1$ cycles among its used states
(C) If there are no cycles among its used states
(D) If there are no cycles among its unused states
43. A PLA consists of two-level $\qquad$ circuits on a single chip.
(A) AND-OR
(B) NOR-NAND
(C) XOR-AND
(D) OR-NAND
44. In which of the following types of counters, the flip-flops do not change states at exactly the same time?
(A) Decade counter
(B) Asynchronous counter with MOD $<2^{\text {n }}$
(C) Asynchronous ripple counter
(D) Cascading asynchronous counter
45. The number of states through which the counter goes is also known as
$\qquad$
(A) Counter
(B) Latch circuit
(C) Multiplexer
(D) MOD number
46. A digital communication system is used to transmit messages, which are in the
$\qquad$ form.
(A) Digital
(B) Analog
(C) Both (A) and (B)
(D) None of the above
47. It contains an equal resistor or current source segment for each possible value of DAC output.
(A) Hybrid DAC
(B) Binary weighted DAC
(C) Segmented DAC
(D) R-2R Ladder DAC
48. The total current can be converted into the corresponding voltage by using an
$\qquad$ —.
(A) $\mathrm{Op}-\mathrm{Amp}$
(B) Binary weighted ladder
(C) Delta sigma DAC
(D) Hybrid DAC
49. The number of resistors required for an N -bit DAC is 2 N in the case of
$\qquad$ _.
(A) Weighted resistor type DAC
(B) Binary weighted DAC
(C) Segmented DAC
(D) R-2R ladder DAC
50. The characteristics of a DAC, which are generally specified by the manufacturers
(A) Linearity
(B) Resolution
(C) Accuracy
(D) All of the above
51. To start the conversion in successive approximation DAC the programmer sets the MSB to $\qquad$ and all other bits to $\qquad$ .
(A) 0,0
(B) 0,1
(C) 1,0
(D) 1,1
52. The major block(s) of the dual- slope ADC
(A) Integrator
(B) Comparator
(C) Binary counter, switch drive
(D) All of the above
53. A counter with 10 states
(A) Cascading asynchronous counter
(B) Decade counter
(C) Asynchronous ripple counter
(D) Ripple counter
54. In asynchronous flip-flop, $\qquad$ and clear pin shows negation.
(A) Bubble at the rest
(B) Active low preset
(C) Clear input
(D) Active high preset
55. It is a single input version of J-K flip-flop formed by tying both the inputs of J-K.
(A)D flip-flop
(B) S flip-flop
(C) T flip-flop
(D) N flip-flop
56. In flip-flop the $\qquad$ arrow shows positive transition on the clock.
(A) Upward
(B) Downward
(C) Vertical
(D) Horizontal
57. Gated S-R latch is a combination of which latch and gate?
(A) J-K latch and NOR gate
(B) S-R latch and NAND gate
(C) S-R latch and NOR gate
(D) J-K latch and NAND gate
58. Which of the following is the advantage of PLD over ICs?
(A) Short design cycle.
(B) Low development cost
(C) Flexible to experiment
(D) All of the above
59. An AND matrix is used to form $\qquad$ terms.
(A) Minimum
(B) Maximum
(C) Product
(D) Sum
60. In a DAC, the possible number of digital input is $\qquad$ .
(A) Fixed
(B) Not fixed
(C) 4
(D) 2

## Unit 4- Memory Element

(1) An n -bit register has a group of n flip-flops and some logic gates.
(A)Logic Gates
(B) Registers
(C) ROM
(D) None of the above
(2) It does not have any external gate.
(A) Simple Register
(B) Buffers
(C) Memory
(D) RAM
(3) A register can also be used to provide data movements.
(A) Parallel Register
(B) Simple Register
(C) Shift Register
(D) All of the above
(4) There are $\qquad$ basic types of shift registers.
(A) Six
(B) Four
(C) One
(D) Many
(5) This type of register accepts inputs data serially,
(A) PIPO
(B) SIPO
(C) PISO
(D) SISO
(6) This type of register accepts inputs data serially
(A) PIPO
(B) SIPO
(C) PISO
(D) SISO
(7) This type of register accepts inputs data simultaneously and output is also coming out parallel
(A) PIPO
(B) SIPO
(C) PISO
(D) SISO
(8) In this type of register, data can be shifted in either right or left direction by using control signal.
(A) PIPO
(B) SISO
(C) Bi-directional Shift Register
(D) None of the above
(9) In this type of counter, the complement of the output of the last stage of the shift register is fed back to the D input of the first state.
(A) Ring Counter
(B) Johnson Counter
(C) Straight Counter
(D) None of the above
10. In this type of counter, the output of the last stage is connected to the D input of the first stage.
(A) Ring Counter
(B) Johnson Counter
(C) Straight Counter
(D) All of the above
11. A device that exhibits two different stable states and functions as a memory element in a binary system is known as $\qquad$ .
(A) Registers
(B) Flip-Flop
(C) VLSI
(D) Both (B) and (C)
12. The different types of flip-flops are $\qquad$
$\qquad$ and $\qquad$ .
(A) R-S
(B) D, T
(C) $\mathrm{J}-\mathrm{K}$
(D) All of the above
13. The $\qquad$ latch is an asynchronous flip-flop which can be constructed from two NAND gates connected back to back.
(A) R-S
(B) JK
(C) SR NOR
(D) None of the above
14. Memory is a circuit, which is used to store $\qquad$ information.
(A) Accurate
(B) Discrete
(C) Analog
(D) Digital
15. This is the minimum length of the write pulse.
(A) Data Set Up Time (tDW)
(B) Data Hold Time (tDH)
(C) Write Pulse Time ( tW )
(D) None of the above
16. This is the maximum time from the start of the valid address of the read cycle to the time when the valid data is available at the data output.
(A) Read cycle time (tRC)
(B) Access time (tA)
(C) Read to output valid time (tRD)
(D) None of the above
17. A register can be either static or dynamic.
(A) Shift
(B) Parallel
(C) Bit
(D) None of the above
18. Read Only Memory (ROM), as the name suggests, is meant only for
$\qquad$ information from it.
(A) Reading/writing
(B) Writing
(C) Reading
(D) All the above
19. A can be programmed only once after which its contents are permanently fixed as ROM.
(A)PROM
(B) PRAM
(C) SROM
(D) None of the above
20. A memory in which the information stored can be erased and new information is stored is called $\qquad$ -.
(A) Non- Erasable Memory
(B) Erasable Memory
(C) Memory
(D) Both (A) and (B)
21. Memory can be classified on the basis of the $\qquad$ technology used.
(A) Non- Fabrication
(B) Bipolar
(C) Fabrication
(D) None of the above
22. A row decoder decodes the $\qquad$ location.
(A) Row
(B) Column
(C) Row/Column
(D) None of the above
23. In a sequential memory, the words are stored in and out in a sequence.
(A) Write
(B) Read
(C) Write/Read
(D) All of the above
24. A $\qquad$ is a semiconductor memory device used to store information, which is permanent in nature.
(A) Last table
(B) RAM
(C) K- Map
(D) ROM
25. ROMs are well suited for the $\qquad$ manufacturing processes.
(A) LSI
(B) BSL
(C) CLP
(D) LSP
26. Erasing EPROM programming is accomplished by using ultraviolet light that belongs to the UVC range and has a frequency of $\qquad$ .
(A) 254.9
(B) 253.2
(C) 253.7
(D) None of the above
27. The EPROM eraser will emit $\qquad$ light
(A) Fluorescent
(B) LED
(C) Laser
(D) UV
28. $\qquad$ organization is essentially an array of selectively open and closed unidirectional contacts.
(A) ROM
(B) RAM
(C) Computer
(D) All of the above
29. The matrix is formed by connecting one diode along with a switch between each row and column.
(A) $3 * 4$
(B) Diode
(C) $2 * 3$
(D) None of the above
30. The EEPROM chip is physically similar to the chip.
(A) EPROM
(B) Minterm
(C) POS
(D) Either (A) or (B)
31. An n-bit register has a group of $\qquad$ flip-flops and some logic gates.
(A) N
(B) P
(C) 10
(D) 0
32. A register can also be used to provide $\qquad$ - movements.
(A) Bit
(B) Data
(C) Signal
(D) None of the above
33. A memory stores data for processing and the instructions for $\qquad$ .
(A) Result
(B) Execution
(C) Progress
(D) All of the above
34. Number of stored bits per unit area, which determines overall storage capacity and memory cost per bit.
(A) Area Efficiency
(B) Access Time
(C) Power Consumption
(D) None of the above
35. The chip select signal is applied to the $\qquad$ terminal.
(A) Chip
(B) Last
(C) CS
(D) Either (A) or (B)
36. The word to be stored is applied to the data $\qquad$ terminals.
(A) Input
(B) Output
(C) Logic
(D) None of the above
37. The $\qquad$ of the desired memory location is applied to the address input terminals.
(A) Name
(B) Address
(C) Number
(D) Level
38. A $\qquad$ command signal is applied to the write-control input terminal.
(A) Write
(B) Read
(C) Write/Read
(D) Both (A) and(B)
39. A PROM can be programmed only once after which its contents are permanently fixed as $\qquad$ _.
(A) ROM
(B) RAM
(C) Memory
(D) Input Data
40. In a sequential memory, the words are stored in and read out in a $\qquad$ .
(A) Parallel
(B) Sequence
(C) Length
(D) None of the above

